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Azizkandi, Mahmoodreza Eskandarpour; Sedaghati, Farzad; Shayeghi, Hossein; Blaabjerg, Frede

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A High Voltage Gain DC-DC Converter Based on Three Winding Coupled Inductor and Voltage Multiplier Cell

Mahmoodreza Eskandarpour Azizkandi, *Student Member, IEEE*, Farzad Sedaghati, Hossein Shayeghi, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*

***Abstract*- This paper introduces a single-switch, high step-up, DC-DC converter based on coupled-inductor (CL) with three winding and voltage multiplier cell (VMC) to obtain a very high voltage conversion ratio. A passive clamp circuit is applied in the converter to recycle the energy of leakage inductance and reduce voltage stress of the main power switch. This leads to utilize a power switch with low on-state resistance and low voltage-rating that decreases the conduction losses. Several advantages include low operating duty cycle, high voltage conversion ratio, low turn ratio of the coupled inductor, leakage inductance reverse recovery, reduced voltage stress of semiconductors, alleviation of diodes reverse recovery issue and high efficiency make the presented topology appropriate for sustainable energy applications such as photovoltaic systems. The operation principle and steady-state analysis of the suggested topology in continuous conduction mode (CCM) are expressed in detail. Also, design procedure and theoretical efficiency analysis of the proposed topology are presented. Moreover, a comparison study is performed to demonstrate the superiority of the presented converter over several similar recently proposed DC-DC converters. Finally, the proposed DC-DC converter feasibility and performance are justified through fabricated 216 W laboratory prototype at 50 kHz switching frequency.**

I. INTRODUCTION

Nowadays, high step-up DC-DC converters have a significant role in sustainable energy applications include photovoltaic (PV) systems, wind power, fuel cells (FCs), etc. In order to decrease problems such as air and environmental pollution and global warming that have been emerged by using fossil fuels, sustainable energy resources are applied to produce electric power. However, the produced DC voltage level of resources such as PV and FCs are low so it is not suitable for connecting to the grid. According to the above mentioned problem, high step-up DC-DC converters are required to increase the output DC voltage level of such resources [1]. How to step up voltage conversion ratio, decrease the semiconductors voltage stress, and enhance the conversion efficiency of the high step-up DC-DC converters constitutes the major concerning issues.

Recently, most of the growths in the installed renewable energy resources systems have been allocated to the grid-connected systems market compared to the off-grid market. Moreover, for example in PV systems, compared with either line frequency or high frequency transformers, the transformer-less PV system has typically a higher-efficiency and reliability, as well as lower complexity and manufacturing cost. Besides, it is worth noting that, the PV module must be grounded in most standards in order to eliminate common mode current. One convenient way to reach this goal is to implement a common grounded transformer-less inverter. In order to eliminate common mode current in grounded PV systems, the step-up DC-DC converter should allow a shared ground between the PV ground and the grid neutral line [2, 3].

In the actual systems having high voltage gain helps DC-DC converters to operate in a very suitable duty cycle. It is important to note that when a DC-DC converter operates in very large duty cycles, the conduction period of power switches and diodes of the converter will be increased. Therefore, the conduction losses of the switching devices will be increased which results in high power losses in the actual systems [4]. Thus, high step-up converters with high efficiency are needed. Moreover, the large duty cycle not only induces very large voltage spikes and increases conduction losses but also induces severe diode reverse-recovery problem [5].

Recently, various step-up DC-DC converters with several techniques of voltage boosting have been presented [6]. Isolated converters have a high voltage conversion ratio due to utilizing transformers with large turn ratio. However, too large turn's ratio leads to a large leakage inductance, which decreases the converter efficiency and increases the switch voltage stress [7, 8]. Moreover, when the galvanic isolation is not needed in the power grid, the conventional boost converter appears as a first choice in boosting the voltage gain due to its low cost and simple structure. However, low voltage conversion ratio, high voltage stress on semiconductors and reverse recovery issues are the basic problems of this converter in high power applications. Moreover, another solution to boost voltage gain is the switched inductor (SI) and switched capacitor (SC) DC-DC converters [9-10]. These

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M. Eskandarpour Azizkandi, F. Sedaghati and H. Shayeghi are with the Department of Electrical and Computer Engineering, University of Mohaghegh Ardabili, Ardabil, Iran (emails: m.eskandarpour@student.uma.ac.ir; farzad.sedaghati@uma.ac.ir; hshayeghi@gmail.com).

F. Blaabjerg is with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (email: fbl@et.aau.dk).

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converters have been utilized widely to obtain high voltage conversion ratio. However, more components are required for extremely high voltage gain, resulting in higher cost and complex circuits. Also, in SI topologies, the voltage stress on semiconductors is high, and in the SC converters, the current stress of semiconductors is high, causing serious conduction losses.

Recently, coupled-inductor (CL) technique with the performance of recycling energy of leakage inductance is extended to increase voltage conversion ratio; therefore, many high step-up CL based converters with characteristics of low voltage stress, high voltage gain and high efficiency have been proposed [11-26]. This type of converters has low reverse recovery ringing of the output diode due to their secondary leakage inductance. Moreover, it is worth noting that using a higher turn ratio and extremely higher duty cycle to achieve a higher voltage gain cause to higher EMI noise and power losses. Recently, several high step-up DC-DC converters based on CL with three winding have been suggested in [27-31], which leads to having more flexible regulation on voltage stress and voltage gain. However, the voltage gain is still not high enough and could be further.

This paper presents a high step-up non-isolated DC-DC converter with three winding CL, which adopts a single power switch. The integration of voltage multiplier cell (VMC) and a CL in the structure of the suggested topology leads to having a very high voltage conversion ratio. The CL can be utilized to step up the static gain, and the VMC offers extra voltage gain. Also, by using a three winding CL, more flexible regulation of the voltage stress and voltage gain on each semiconductor component is obtained. A passive voltage clamp circuit is utilized in the converter to recycle the CL energy and clamp the voltage on the main power switch. This results in selecting a switch with low on-state resistance and low voltage-rating in the converter to decline the conduction loss. Several advantages of the suggested topology such as achieving high voltage conversion ratio in low duty cycles by utilizing low turn ratio of the CL, smaller leakage inductance due to low number of turns, alleviation of reverse recovery issue of diodes due to operating in low duty cycles, utilization of only one power switch, low conduction losses, reduced voltage stress on semiconductors, leakage inductance energy recovery and high efficiency make it appropriate for sustainable energy applications such as PV's and FCs. The operational principle and steady-state analysis of the suggested converter are presented in the following section.

II. Operation Principle and Steady-State Analysis of Proposed DC-DC Converter

The equivalent power circuit of the suggested DC-DC converter is indicated in Fig. 1. As illustrated in this figure, the presented topology consists of a power switch S, four capacitors C_1-C_4, four diodes D_1-D_4, one coupled inductor with three windings, output filter capacitor C_O and output diode D_O. The coupled inductor with three winding is modeled as an ideal transformer with a turn ratio N_1: N_2: N_3, a leakage inductance, L_{Lk} and a magnetizing inductance, L_m. N_1, N_2 and

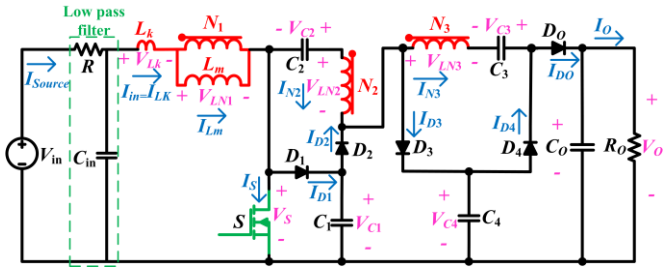

Fig. 1. Equivalent power circuit of the suggested DC-DC converter.

N_3 are the ideal transformer primary, secondary and tertiary windings turn numbers, respectively. Also, the coupled inductor turn's ratio is presumed as $n_2=N_2/N_1$ and $n_3=N_3/N_1$. The capacitor C_1 and diode D_1 operate as clamp circuit components to recycle the leakage inductance energy. Capacitor C_2 is employed as a voltage lift capacitor and also, the tertiary side of coupled inductor, capacitors C_3 and C_4 and diodes D_3 and D_4 operate as a voltage multiplier cell (VMC) to increase the converter voltage gain.

To simplify the circuit analysis in the suggested structure, some assumptions are presumed in the following:

-All capacitors are large enough. Thus, voltages V_{C1}-V_{C4} are presumed to be constant in one period.

-All components are considered to be ideal.

-The leakage inductance is considered and the coupling coefficient of coupled inductor, k, is equal to $L_m/(L_m+L_k)$.

The operation principle of the suggested topology in continuous conduction mode (CCM) includes five time intervals. Fig. 2 indicates the current flow path of the presented topology at several operating modes, and also, the main waveforms of the converter operation in CCM are illustrated in Fig. 3. The five modes are expressed as follows:

Mode 1 [t_0, t_1]: At the beginning of the first mode, the power switch S starts to conduct, and diodes D_3 and D_O are conducting and diodes D_1, D_2 and D_4 are blocked. During this short time transition, as the current of leakage inductance, I_{LK}, increases linearly, the currents of the tertiary and secondary side of the coupled inductor, I_{N3} and I_{N2}, decrease linearly. According to Fig. 2(a), the capacitor C_4 is charged through the diode D_3, and capacitors C_2 and C_3 are discharged and their energies are delivered to the load and capacitor C_O. This state finishes when the current of the leakage inductance equals to the magnetizing inductance current and diodes D_3 and D_O turned off. For the coupled inductor with three windings, we have:

$$N_1 I_{N1} = N_2 I_{N2} + N_3 I_{N3} \Rightarrow I_{N1} = n_2 I_{N2} + n_3 I_{N3} \quad (1)$$

Mode 2 [t_1, t_2]: In the second mode, the power switch S is still conducting and diodes D_1, D_3 and D_O are blocked and diodes D_2 and D_4 turn on, as indicated in Fig. 2(b). In this mode, the leakage and magnetizing inductances are charged by the input source, and their current, I_{Lm} and I_{Lk}, increase linearly. The voltage of series-connected capacitor C_1 and winding N_2, V_{C1} and V_{N2}, charges the capacitor C_2 via the diode D_2 and the main power switch. Meanwhile, the voltage of series-connected winding N_3 and capacitor C_4, V_{N3} and V_{C4}, charges the capacitor C_3 via the diode D_4. Moreover, in this state, the

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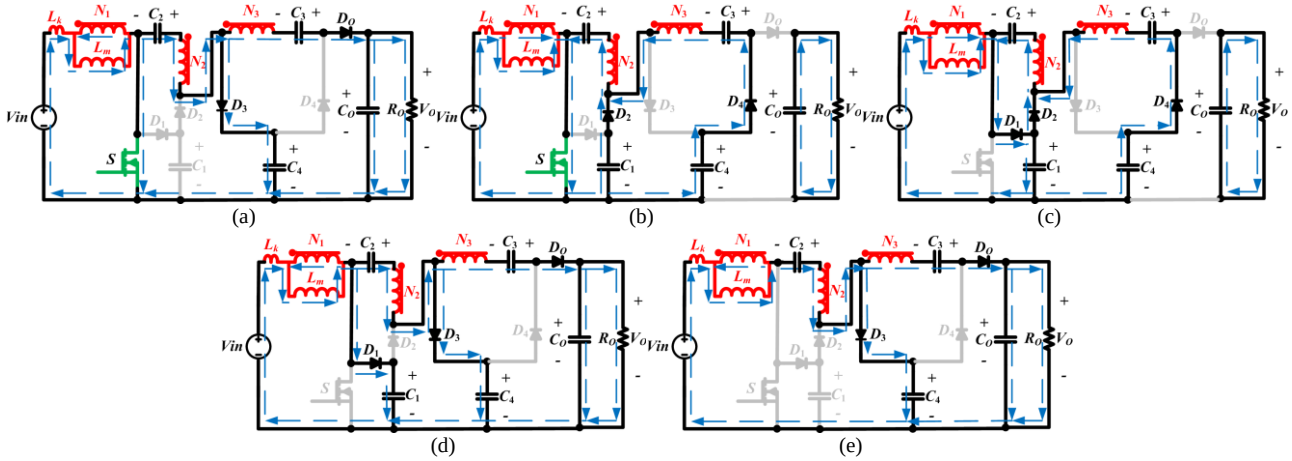

Fig. 2. Current flow path of presented converter in one period at CCM operation: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, and (e) Mode 5.

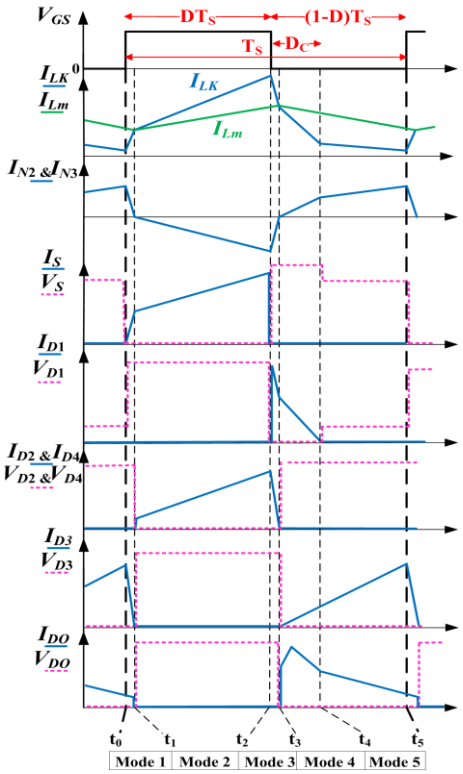

Fig. 3. Main waveforms of the suggested converter in CCM operation.

capacitor C_O supplies the load. This time transition finishes when the main power switch is blocked. In this state, the following equations can be achieved by applying Kirchhoff's Voltage Law (KVL) on the circuit:

$$V_{Lm} = [L_m / (L_m + L_k)]\, v_{in} = kV_{in} \tag{2}$$

$$V_{Lk} = [L_k / (L_m + L_k)]\, v_{in} = (1-k)V_{in} \tag{3}$$

$$V_{LN2} = V_{C2} - V_{C1} = n_2 k V_{in} \tag{4}$$

$$V_{LN3} = V_{C1} - V_{C4} + V_{C3} = n_3 k V_{in} \tag{5}$$

Mode 3 [t_2, t_3]: From the time t=t_2, as illustrated in Fig. 2(*c*), switch S is turned off, and diodes D_1, D_2 and D_4 are conducting and diodes D_3 and D_O are blocked. During this short state, the leakage inductance is demagnetized. Therefore, the leakage inductance energy is recycled to the capacitor C_1 and charges it through the diode D_1. Meanwhile, the currents of windings N_3 and N_2, I_{N3} and I_{N2}, are declined quickly since the contrary direction of the voltage of the windings N_3 and N_2. In this mode, capacitor C_2 is charged by the winding N_2 through diodes D_1 and D_2. Moreover, capacitor C_3 is still charged through the capacitor C_4 and the winding N_3. Also, the capacitor C_O energy is delivered to the load. This stage finishes, when the currents I_{Lk} and I_{Lm} become equal.

Mode 4 [t_3, t_4]: In the fourth mode, switch S is still in off-state, and diodes D_1, D_3 and D_O are in on-state and diodes D_2 and D_4 are blocked. In this stage, since the currents of leakage and magnetizing inductances, I_{Lk} and I_{Lm}, decrease linearly, the currents of secondary and tertiary windings, I_{N2} and I_{N3}, are increased linearly according to principle of the ideal transformer. Recycling the leakage inductance energy is continued in this state too, and the capacitor C_1 is charged through diode D_1. Moreover, the capacitor C_4 is charged through the diode D_3. Also, the input voltage source, V_{in}, and capacitors C_2 and C_3 provide the energy of the load and charge the output capacitor C_O. When the diode D_1 is blocked at time t=t_4, this time interval finishes. As shown in Fig. 2(*d*), the following equations can be achieved for this mode:

$$V_{Lm} = k(V_{in} - V_{C1}) \tag{6}$$

$$V_O = V_{C3} + V_{C4} - V_{LN3} = V_{C3} + V_{C4} - n_3 k(V_{in} - V_{C1}) \tag{7}$$

Mode 5 [t_4, t_5]: As indicated in Fig. 2(*e*), in the last state, the switch S is still off and diodes D_3 and D_O are conducting and diodes D_1, D_2 and D_4 are reverse biased. In this mode, the leakage and magnetizing inductance currents decrease linearly, too. Also, the capacitor C_4 is still charged through diode D_3. Moreover, the energy of the input source and magnetizing inductance along with capacitors C_2 and C_3 are delivered to the capacitor C_O and load. This time transition ends by turning on the main power switch anew, and the next switching period begins. Moreover, in this mode, the voltage across the L_m is determined by using the following equation:

$$V_{Lm} = V_{in} - V_{C4} - kn_2 V_{in} + kn_2 V_{C1} + V_{C2} \tag{8}$$

The voltage of capacitor C_4, V_{C4}, is obtained as follows:

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$$V_{C4} = (1-k)V_{in} + kV_{C1} - kn_2V_{in} + kn_2V_{C1} + V_{C2} \quad (9)$$

To simplify steady-state analysis of the converter, only Modes 2, 4 and 5 are considered because the time transitions of Modes 1 and 3 are significantly short. Therefore, by using the inductor volt-second balance law for the L_m, the voltage across capacitor C_1 is achieved as follows:

$$V_{C1} \approx [V_{in} / (1-D)] \quad (10)$$

Where D is the duty cycle of switch.

According to (4) and (10), the voltage across capacitor C_2 is derived as given in (11).

$$V_{C2} = [(kn_2 - kn_2D + 1)V_{in} / (1-D)] \quad (11)$$

By substituting (10) and (11) into (9), the voltage across capacitor C_4 is equal to (12).

$$V_{C4} = [((kn_2 + 1 + k + (1-k)(1-D))V_{in}) / (1-D)] \quad (12)$$

From (5) and also, by using (10) and (12), the voltage across capacitor C_3 is achieved as follows:

$$V_{C3} = [((kn_2 + kn_3 - kn_3D + k + (1-k)(1-D))V_{in}) / (1-D)] \quad (13)$$

From (7), (10), (12) and (13), the voltage gain of the suggested converter in CCM, M_{CCM}, is achieved as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = [\frac{(2k + 1 + 2kn_2 + (2(1-k)(1-D)) + n_3k)}{(1-D)}] \quad (14)$$

Fig. 4(a) indicates the voltage gain versus duty cycle with considering the effect of leakage inductance under different coupling coefficients, where the turns ratio is set to be n_2=2 and n_3=1. It is evident that the coupling coefficient does not have a significant effect on the voltage gain. Hence, if the coupled inductor leakage inductance is not considered, it means the coupling coefficient k is equal to 1 and the suggested converter ideal voltage gain is determined as follows:

$$M_{CCM} = V_O / V_{in} = [(3 + 2n_2 + n_3) / (1-D)] \quad (15)$$

In order to simplify the analysis of the converter in the next sections, the coupling coefficient k is considered to be 1. Ideal voltage gain of the suggested converter in CCM, M_{CCM}, versus switch duty cycle, D, under different turn ratios of the coupled inductor, n_2 and n_3, are indicated in Fig. 4(b). It can be found that the turn ratios of the coupled inductor, n_2 and n_3, can be adjusted to obtain a very high voltage conversion ratio without applying an extremely large duty cycle and operating at large turn ratios of the coupled inductor.

III. Design Procedure of Proposed Converter

In order to choose the proper power switch and diodes for the suggested topology, current and voltage stresses of these elements should be determined.

A. Current Stress Analysis

According to steady-state analysis, the current ripple of the magnetizing inductance in CCM operation is determined as:

$$\Delta I_{Lm} = [DV_{in} / L_m f_s] = [DV_{in} T_s / L_m] \quad (16)$$

Where f_s is the converter switching frequency.

Moreover, the average current of the magnetizing inductance L_m is achieved as given in (17).

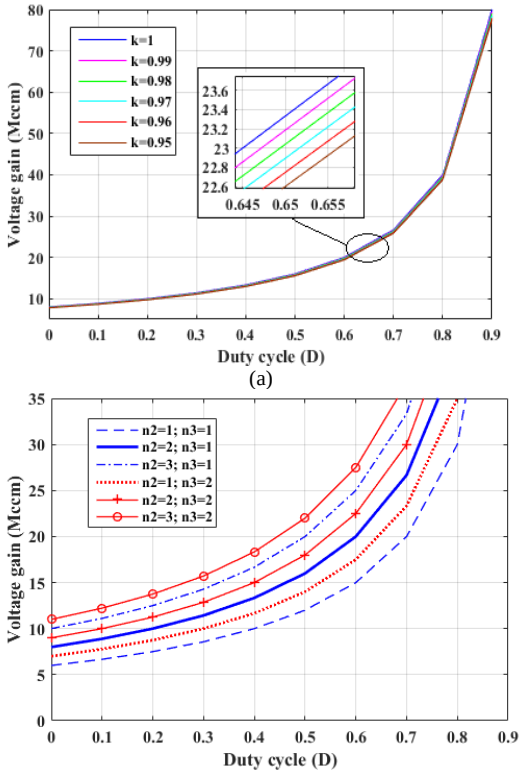

Fig. 4. Voltage gain versus duty cycle (a) under various coupling coefficients, and (b) under several coupled inductor turns ratios.

$$I_{Lm} = I_{in} = [(3 + 2n_2 + n_3)I_O / (1-D)] \quad (17)$$

Thus, the peak value of the magnetic inductance current is derived as follows:

$$I_{Lm}^{(peak)} = \frac{(3 + 2n_2 + n_3)}{(1-D)} I_O + \frac{1}{2} \frac{DV_{in}}{L_m f_s} \quad (18)$$

According to Fig. 3, in terms of the CCM operation steady-state analysis and by using ampere-second balance law on all capacitors, C_1-C_4 and C_O, the average currents of all diodes are equal to the output current, I_O. Hence, the value of diodes peak current and the main power switch can be determined as follows:

$$I_{D_2}^{(peak)} = I_{D_4}^{(peak)} = [2I_O / D] \quad (19)$$

$$I_{D_3}^{(peak)} = I_{D_O}^{(peak)} = [2I_O / (1-D)] \quad (20)$$

$$I_{switch}^{(peak)} = \left[\frac{4 - D + (2n_2 + n_3)(2-D)}{D(1-D)}\right] I_O + \frac{1}{2} \frac{DV_{in}}{L_m f_s} \quad (21)$$

According to Fig. 3, based on capacitor C_2 charge balance, the time transition of Mode 4, D_C , is achieved as follows:

$$D_C = [2(1-D) / (2 + 2n_2 + n_3)] \quad (22)$$

Therefore, by using (22), the peak value of diode D_1 current, $I_{D_1}^{(peak)}$, is obtained as given in (23).

$$I_{D_1}^{(peak)} = \frac{2\langle i_{D_1} \rangle}{D_C} = \frac{2I_O}{D_C} = \frac{(2 + 2n_2 + n_3)I_O}{(1-D)} \quad (23)$$

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B. Voltage Stress Analysis

According to the converter operation principle, the voltage stress of semiconductor components are calculated as given in (24)-(26).

$$V_{stress-S_1} = V_{stress-D_1} = \frac{1}{(1-D)}V_{in} = \frac{1}{(3+2n_2+n_3)}V_O \quad (24)$$

$$V_{stress-D_{2,3}} = \frac{(1+n_2)}{(1-D)}V_{in} = \frac{(1+n_2)}{(3+2n_2+n_3)}V_O \quad (25)$$

$$V_{stress-D_{4,O}} = \frac{(1+n_2+n_3)}{(1-D)}V_{in} = \frac{(1+n_2+n_3)}{(3+2n_2+n_3)}V_O \quad (26)$$

C. Magnetizing inductance design

In order to guarantee the operation of the suggested converter in CCM, the average current through the magnetic inductance, I_{Lm}, must be higher than half of the current ripple of magnetic inductance, ΔI_{Lm}. The continuity of the magnetizing current is also considered in the design of the magnetizing inductance. Therefore, by using (16) and (17), the magnetizing inductance minimum value for the presented converter is obtained as follows:

$$L_m \geq [D(1-D)^2 R_O / 2fs(3+2n_2+n_3)^2] \quad (27)$$

According to (27), magnetizing inductance must be more than 15 µH. Thus, to guarantee CCM operation of the implemented prototype, a coupled inductor that has a 100 µH magnetizing inductance is applied.

D. Capacitors design

In order to suppress the capacitors voltage ripple, the minimum capacitance should be determined. All capacitors are designed by assuming the same voltage ripple. According to (10)-(13), the voltages of capacitors C1-C4 for the proposed topology are achieved. Since the charge absorbed or produced by all capacitors are equal, and according to $\Delta Q = C\Delta V_C = I_C \Delta T$, the size of the capacitors are derived as given in (28) and (29).

$$C_i \geq [V_O / \Delta V_{Ci} R_O f_S] \quad (28)$$

$$C_O \geq [DV_O / \Delta V_{CO} R_O f_S] \quad (29)$$

where i=1, 2, 3 and 4.

Some power is dissipated when the equivalent series resistance (ESR) of capacitor is considered. As the capacitance of an aluminum electrolytic capacitor increases, its ESR will be smaller. So, in general, the capacitance is chosen to be much larger than the calculated value. The sizes of the capacitors that are employed in the implemented prototype satisfy the equations derived in (28) and (29).

IV. Comparison of the Proposed Converter

To demonstrate merits of presented converter and confirm its performance, some comparisons are discussed in this section. The main features of the suggested converter and similar coupled inductor based converters using a single switch recently presented in [9], [15-31] are indicated in Table I. As demonstrated in this table, with considering the voltage gain, besides that the component number of the suggested converter is equal to the converters presented in [18-21], [27, 28] and [30], the voltage gain of the suggested topology is higher than them. Moreover, it is worth noting that the voltage gain of the converters suggested in [15-17], [24] and [31] is lower than the proposed converter with more numbers of power components. Although, the component number of the converters presented in [9, 22, 23, 25, 26] and [29] is lower than the proposed converter. However, their voltage gain is remarkably lower than the presented structure. Moreover, between the input and output of the suggested structure, there is a common ground connection, which is a very important factor for a step-up front-end DC-DC module of a transformer-less grid-tied inverter.

According to Fig. 5, the voltage gain of the suggested topology is greater than the topologies presented in [9] and [15-31] for all ranges of duty cycle with n_2=2 and n_3=1. This advantage is due to the integration of a three-winding coupled inductor with the VMC in the suggested structure. As indicated in Fig. 6(a), the main switch normalized voltage stress in the presented topology is less than the other topologies for any values of the duty cycle.

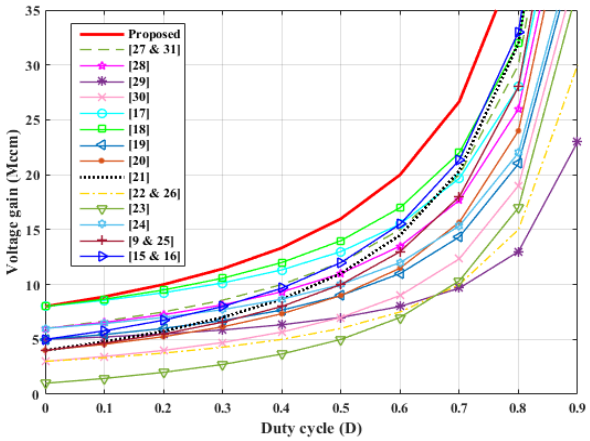

Fig. 5. Voltage gain comparison of several boost converters. (n_2=2, n_3=1)

Moreover, Fig. 6(b) illustrates the normalized voltage stress across the output diode that has the maximum voltage stress in the high step-up converters. As indicated in this figure, the normalized output diode voltage stress in the presented converter is less than the topologies presented in Table I for any values of the duty cycle (even in [15-18] and [24]). Also, converters in [15-18] and [24] have less normalized output diode voltage stress than the suggested converter. However, they have also more components, higher switch voltage stress and lower voltage gain than the suggested converter.

Finally, according to the comparison study, the proposed converter has a remarkably higher voltage gain over other high step-up converters due to integrating three-winding CL, voltage lift capacitor (C_2) and VMC network. Also, utilizing a three winding CL in the structure of the converter results in more flexible regulation of the voltage conversion ratio and voltage stress on each semiconductor component. Having an ultra large conversion ratio causes to operate proposed

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TABLE I. COMPARISON OF THE PRESENTED DC-DC CONVERTER WITH SEVERAL OTHER SIMILAR TOPOLOGIES.

Reference	Number of Components				Voltage gain	Voltage stress on main switch	Voltage stress of output diode(s)	C-g
	D	C	S	CL+L				
Proposed converter	5	5	1	$1^{3w}+0$	$(3+2n_2+n_3)/(1-D)$	$V_O/(3+2n_2+n_3)$	$(1+n_2+n_3)V_O/(3+2n_2+n_3)$	Y
Converter in [27]	5	5	1	$1^{3w}+0$	$(3+n_2+n_3)/(1-D)$	$V_O/(3+n_2+n_3)$	$(1+n_2+n_3)V_O/(3+n_2+n_3)$	N
Converter in [28]	6	6	1	$1^{3w}+0$	$(2+n_2+n_3(2-D))/(1-D)$	$V_O/(2+n_2+n_3(2-D))$	$(1+n_2+n_3)V_O/(2+n_2+n_3(2-D))$	Y
Converter in [29]	4	4	1	$1^{3w}+0$	$(2+n_2+n_3-(1+n_2)D)/(1-D)$	$V_O/(2+n_2+n_3-(1+n_2)D)$	$(1+n_2)V_O/(2+n_2+n_3-(1+n_2)D)$	Y
Converter in [30]	5	5	1	$1^{3w}+0$	$(1+n_2+n_3D)/(1-D)$	$V_O/(1+n_2+n_3D)$	$(n_2)V_O/(1+n_2+n_3D)$	Y
Converter in [31]	6	5	2	$2^{3w}+0$	$2(N+1)/(1-D)$	$V_O/2(N+1)$	$(2N+1)V_O/2(N+1)$	Y
Converter in [17]	8	8	1	$1^{2w}+1$	$(4+n_2(2-D)-D)/(1-D)$	$V_O/(4+n_2(2-D)-D)$	$(n_2(2-D)-D)V_O/(4+n_2(2-D)-D)$	Y
Converter in [18]	5	5	1	$1^{2w}+0$	$(2+n_2(3-D))/(1-D)$	$V_O/(2+n_2(3-D))$	$(1+n_2)V_O/(2+n_2(3-D))$	Y
Converter in [19]	4	5	1	$1^{2w}+1$	$(1+D+n_2(2-D))/(1-D)$	$V_O/(1+D+n_2(2-D))$	$(1+n_2)V_O/(1+D+n_2(2-D))$	Y
Converter in [20]	4	5	1	$1^{2w}+1$	$(2+n_2+D)/(1-D)$	$V_O/(2+n_2+D)$	$(1+n_2)V_O/(2+n_2+D)$	Y
Converter in [21]	4	5	1	$1^{2w}+1$	$(2+n_2+(n_2+1)D)/(1-D)$	$V_O/(2+n_2+(n_2+1)D)$	$(1+n_2)V_O/(2+n_2+(n_2+1)D)$	Y
Converter in [22]	2	3	1	$1^{2w}+1$	$(1+n_2)/(1-D)$	$V_O/(1+n_2)$	V_O	Y
Converter in [23]	2	3	1	$1^{2w}+1$	$(1+(n_2+1)D)/(1-D)$	$V_O/(1+(n_2+1)D)$	$(1+n_2)V_O/(1+(n_2+1)D)$	Y
Converter in [24] ($BCI^{SC(D)+VM}$)	6	6	1	$1^{2w}+0$	$(2+n_2D+2n_2(1-D))/(1-D)$	$V_O/(2+n_2D+2n_2(1-D))$	$(n_2)V_O/(2+n_2D+2n_2(1-D))$	Y
Converters in [9 & 25]	4	4	1	$1^{2w}+0$	$(2+n_2+n_2D)/(1-D)$	$V_O/(2+n_2+n_2D)$	$(1+n_2)V_O/(2+n_2+n_2D)$	Y
Converter in [26]	3	4	1	$1^{2w}+1$	$(1+n_2)/(1-D)$	$V_O/(1+n_2)$	$(n_2)V_O/(1+n_2)$	Y
Converters in [15&16]	6	6	1	$1^{2w}+0$	$1+2n_2+n_2D/(1-D)$	$V_O/1+2n_2+n_2D$	$(n_2)V_O/1+2n_2+n_2D$	Y

D=Diode; C=Capacitor; S=Switch; CL=Coupled Inductor; L=Inductor; 3w=3-winding; 2w=2-winding; C-g: Common grounded; Y: Yes; N: No

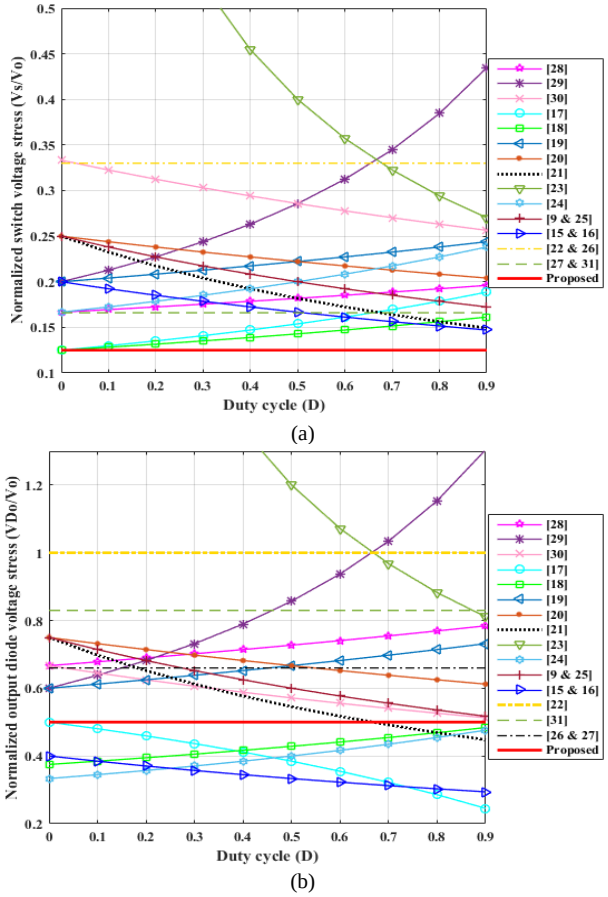

Fig. 6. Characteristics of boost converters: (a) Power switch normalized voltage stress, and (b) output diode normalized voltage stress. (n_2=2, n_3=1)

converter in very suitable duty cycles. Moreover, it is demonstrated that the normalized voltage stress of the main switch and output diode of the proposed converter is lower than the other high step-up converters. This attractive feature causes to utilize a power switch with low $R_{DS(on)}$ resistance and voltage rating in the power circuit of the proposed converter to decrease the cost and enhance the efficiency. Furthermore, the proposed converter has a common ground connection between input and output, which is a very important factor for a step-up DC-DC converter.

V. EFFICIENCY ANALYSIS OF THE PROPOSED CONVERTER

In order to do the presented converter efficiency analysis, parasitic resistances are considered and defined as follows: $R_{\text{DS-on}}$ is on-state resistance of the switch, R_{LN1}, R_{LN2} and R_{LN3} are the equivalent series resistance (ESR) of primary, secondary and tertiary side of coupled inductor respectively. R_{FD1}-R_{FD4} and R_{FDO} are diodes D_1-D_4 and D_O forward resistances, respectively, and V_{FD1}-V_{FD4} and V_{FDO} are their threshold voltages. Also, r_{C1}-r_{C4} and r_{CO} are the capacitors C_1-C_4 and C_O ESR, respectively. Thus, the calculated efficiency of the converter is formulated as given in (30) and (31).

$$\eta = [P_O/(P_O + P_{loss})] \times 100 \quad (30)$$

$$P_{loss} = A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 \quad (31)$$

Where A_1 is conduction loss of the switch in the presented converter and can be derived as follows:

$$A_1 = R_{DS-on} \times \left(\sqrt{D}\left(\frac{4-D+(2n_2+n_3)(2-D)}{D(1-D)} I_O + \frac{DV_{in}}{L_m f_s}\right)\right)^2 \quad (32)$$

A_2 is the converter switching loss, and it is equal to:

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$$A_2 = (0.5) f_S I_S V_S (t_{on} + t_{off}) \quad (33)$$

where t_{on} and t_{off} are rise and fall times of the switch that are given by device static characteristics provided by manufacture datasheet information, I_S is the switch current during the switching time and V_S is the switch maximum voltage stress.

A_3 is the diodes forward resistance loss of the converter and can be calculated as given in following:

$$A_3 = R_{FD1} * \left[\frac{\sqrt{D_C}\,(2+2n_2+n_3) I_O}{(1-D)} \right]^2 + (R_{FD2} + R_{FD4}) * \left[\frac{2I_O}{\sqrt{D}} \right]^2 + (R_{FD3} + R_{FDO}) * \left[\frac{2I_O}{\sqrt{1-D}} \right]^2 \quad (34)$$

A_4 is the diodes forward voltage loss and equals to:

$$A_4 = V_{FD1-4,O} \times I_{D1-4,O_{(ave)}} = I_O (V_{FD1} + V_{FD2} + V_{FD3} + V_{FD4} + V_{FDO}) \quad (35)$$

A_5 is the power losses of the capacitors of the converter, which can be determined as given in (36).

$$A_5 = r_{C1,2,3,4,O} \times (I^2_{rms,C1,2,3,4,O}) \quad (36)$$

A_6 is the conduction loss of the primary, secondary and tertiary sides of the coupled inductor in the converter that can be formulated as:

$$A_6 = R_{LN1} * (I^2_{rms,LN1}) + R_{LN2} * (I^2_{rms,LN2}) + R_{LN3} * (I^2_{rms,LN3}) \quad (37)$$

Finally, A_7 is the core losses of the coupled inductor that can be determined with the Steinmetz equations and expressed as:

$$A_7 = K f^{\alpha} (B_{\max})^{\beta} A_c l_c \quad (38)$$

where A_c is a cross sectional area of the core, l_c is the mean path length of the core and B_{max} is the peak flux density. Typically values of K, α, and β are provided in the datasheet by the manufactures.

Moreover, the voltage gain of the suggested converter including the conduction losses can be determined as follows:

$$M_{CCM} = [\eta(3 + 2n_2 + n_3) / (1 - D)] \quad (39)$$

VI. Experimental Results Analysis

In order to justify the feasibility and verify the theoretical analysis of suggested converter, the experimental results of 216 W implemented power circuit of the suggested topology are presented. In all the figures, the time per division is set to be 8 µs. The specifications of the implemented converter are given as follow:

Input voltage: 28 V; Output voltage: 418 V; Output power: 216 W; Duty cycle: 0.50; Switching frequency: 50 kHz; Coupled inductor: EE-55/28/21 ferrite core; L_m=100 uH; $L_k \approx$ 1.5 uH; N_1: N_2: N_3=1: 2: 1; Capacitors type: Electrolytic capacitor; C_1-C_4: 47 uF/250V; C_{in}: 470 uF/63V; C_O: 220 uF/ 450V; Power switch (S): IRFp260n [PD - 94004B] n-channel MOSFET (V_{DSS}=200 V, I_D=50 A, $R_{DS(on)}$=0.04 Ω); Diodes (D_1-D_4 and D_O): MUR1560 ultra-fast diode (V_R=600 V, $I_{F(ave)}$=15 A, V_F=1.2 V);

Experimental measurement results of the converter operation in CCM are given in Fig. 7. As depicted in Fig. 7(a), the measured output and input voltage is about 418 V and 28 V, respectively. According to this figure, the ripple of the output voltage with the output capacitor of 220 µF is very low. As illustrated in Fig. 7(b), the maximum voltage on the main power switch is about 60 V and far lower than the output voltage (about 14% of the output voltage). Thus, a switch with low $R_{DS(on)}$ resistance can be utilized to enhance the overall efficiency. According to Fig. 7(b), the duty ratio of the main switch is close to 0.50. Fig. 7(b) demonstrates that the leakage inductance stored energy is recycled to the capacitor C_1 through diode D_1 (I_{D1}). Fig. 7(a) indicates the input current waveform that is identical with leakage inductance current without an input filter. The ripple of the input current is more than other presented high step-up converters such as the topologies presented in [17], [19-23] and [26]. However, as it is depicted in Fig. 7(a) (I_{Source}), a low pass filter can be utilized to decline the input current ripple. According to Figs. 7(b) and (d), the diodes D_1, D_2 and D_O measured voltage stress are found to be about 60 V, 158 V and 218 V, respectively. It is obvious that the output voltage is far higher than the diodes voltage stresses; hence, ultrafast diodes are employed to alleviate the reverse recovery current. The capacitors C_1-C_4 voltage waveforms are indicated in Fig. 7(c), which are in agreement with (10)-(13). The current in the diodes D_1, D_2 and D_O and switch S are shown in Figs. 7(a) and (d). The obtained results confirm the theoretical waveforms, given in Fig. 3.

Fig. 8(a) shows the measured efficiencies of the suggested converter under several output powers for two different input voltages while the output voltage (V_O) is regulated at 418 V in both conditions. The peak value of the efficiency is 96.2% which is obtained at 180 W when V_{in}=38 V and the measured efficiency of the converter at nominal power is about 94% (V_{in} = 28 V). It can be found that as the input voltage increases, the efficiency of the converter is enhanced.

Fig. 8(b) shows the efficiency comparison of the proposed converter with other similar topologies while keeping the

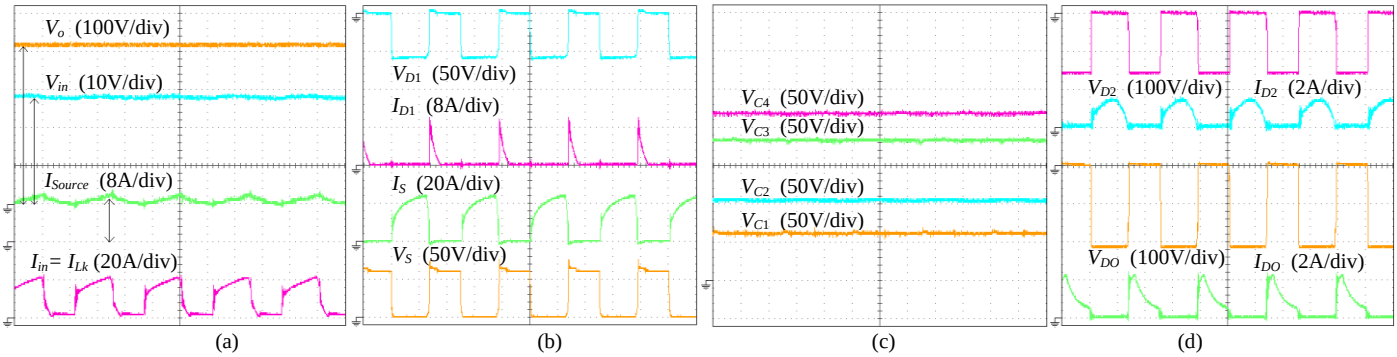

Fig. 7. Experimental results of the implemented converter, (a) V_O, V_{in}, I_{Source}, I_{in}=I_{Lk}, (b) V_{D1}, I_{D1}, I_S, V_S, (c) V_{C3}, V_{C4}, V_{C2}, V_{C1}, and (d) V_{D2}, I_{D2}, V_{DO}, I_{DO}.

output voltage regulation. For a fairly comparison, the simulated results presented in this figure, are based on the same specifications, switching components and conditions (f_S=50kHz, V_{in}=28V and n_2=2 and n_3=1). According to this figure, the proposed converter has better efficiency than others due to having high voltage gain in very suitable duty cycles that results in low power losses.

In fact, the parasitic elements of the implemented converter have a little impact on the voltage gain. The theoretical voltage gain based on (15) and experimental tested voltage gain under V_{in} = 28 V, f_s = 50 kHz, n_2 = 2 and n_3= 1 is indicated in Fig. 9. As illustrated in this figure, the experimental tested voltage gain is a little lower than the theoretically calculated voltage gain due to the parasitic elements.

Finally, according to the experimental results, the feasibility and performance of the suggested converter are confirmed.

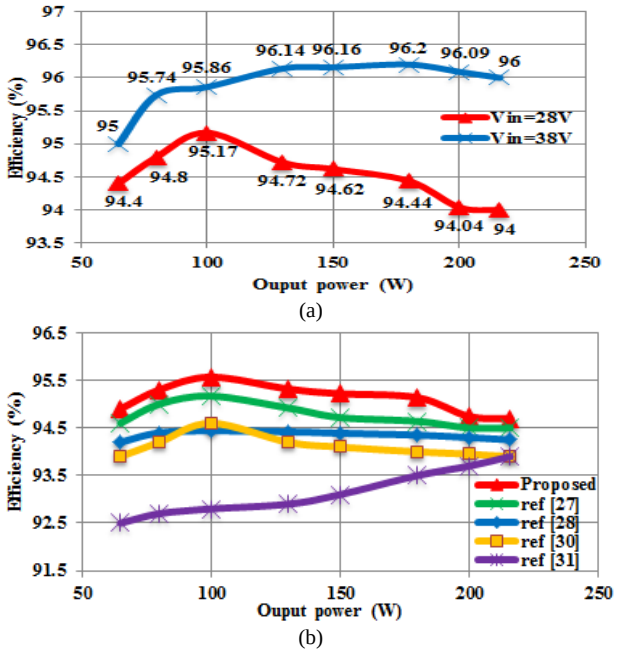

Fig. 8. (a) Measured efficiencies of the presented converter under several output powers for two different input voltages when V_O is regulated at 418 V (f_S = 50 kHz and n_2=2 and n_3=1), and (b) efficiency comparison of the proposed converter with other similar topologies under different power loads.

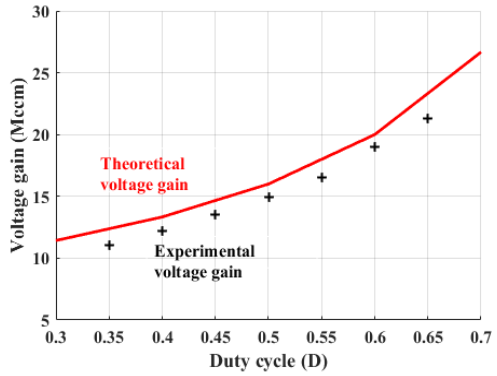

Fig. 9. Theoretical and experimental tested voltage gain under V_{in} = 28 V, f_s = 50 kHz, n_2 = 2 and n_3 = 1.

VII. Conclusion

In this paper, a high step-up three-winding coupled inductor based DC-DC converter with voltage multiplier cell is introduced. High voltage gain in low turn ratios and suitable operating duty cycles, recycled leakage inductance energy, high efficiency and low voltage stress on the switch and diodes are the main merits of the suggested topology. The operational principle and steady-state analysis of the converter under CCM condition has been expressed completely. Moreover, the design procedure and theoretical efficiency analysis of the converter were determined in detail. The superiority of the suggested converter was justified over several high step-up recently proposed coupled inductor based DC-DC converters in the comparison study. Finally, the feasibility of the presented converter was verified through the results of the implemented converter under the output power of 216 W.

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Mahmoodreza Eskandarpour Azizkandi was born in Hashtrood, Iran, in 1993. He received his M.Sc. degree in Power Electronics Engineering from the University of Mohaghegh Ardabili, Ardabil, Iran in 2019. He is currently working toward Ph.D degree in Power Electrical Engineering at Iran University of Science & Technology, Tehran, Iran. He was selected as the prominent graduated student by the Iran National Elites Foundation in May. 2019. His research interests include renewable energy systems, power electronics converters, especially coupled inductor based converters and high step-up DC-DC converters for renewable energy applications.

Farzad Sedaghati was born in Ardabil, Iran, in 1984. He received the M.S. and Ph.D. degrees both in electrical engineering in 2010 and 2014 from the University of Tabriz, Tabriz, Iran. In 2014, he joined the Faculty of Engineering, Mohaghegh Ardabili University, where he has been an Assistant Professor since 2014. His current research interests include renewable energies and power electronic converters design and applications.

Hossein Shayeghi is a full Professor in the Technical Engineering Department of the University of Mohaghegh Ardabili, Ardabil, Iran. His research interests are in the application of robust control, artificial intelligence and heuristic optimization methods to power system control design, operation, and planning, power system restructuring and power electronics design for renewable energies applications. He has authored and co-authored more than 350 papers in international journals and conference proceedings. He has been included in the Thomson Reuters' list of the top one percent of most-cited technical engineering scientists in 2015, 2016, 2017 and 2018, respectively.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1992. He became an Assistant Professor in 1992, an Associate Professor in 1996 and a full professor in power electronics and drives in 1998. From 2017, he became a Villum Investigator. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 500 journal papers in the fields of power electronics and its applications. Dr. Blaabjerg received 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. In 2018, he is President Elect of IEEE Power Electronics Society.